IDEC Chip Design Contest

Low Power SoC with Digital Filter Accelerator for Embedded System

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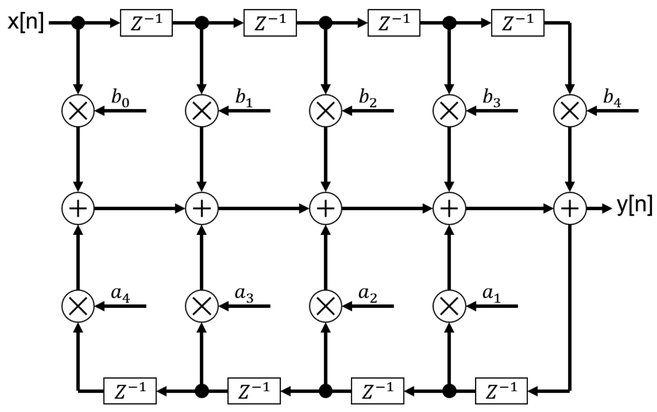
Abstract

As the growing number of wearable devices, the filtering requirements are also on the increase. These digital signal processing tasks are processed by general-purpose digital signal processors. However, these are inappropriate in embedded systems. So we propose a low-power SoC for digital signal processing. We verified our chip by prototype board.

1-order IIR Filter with 4 Channel

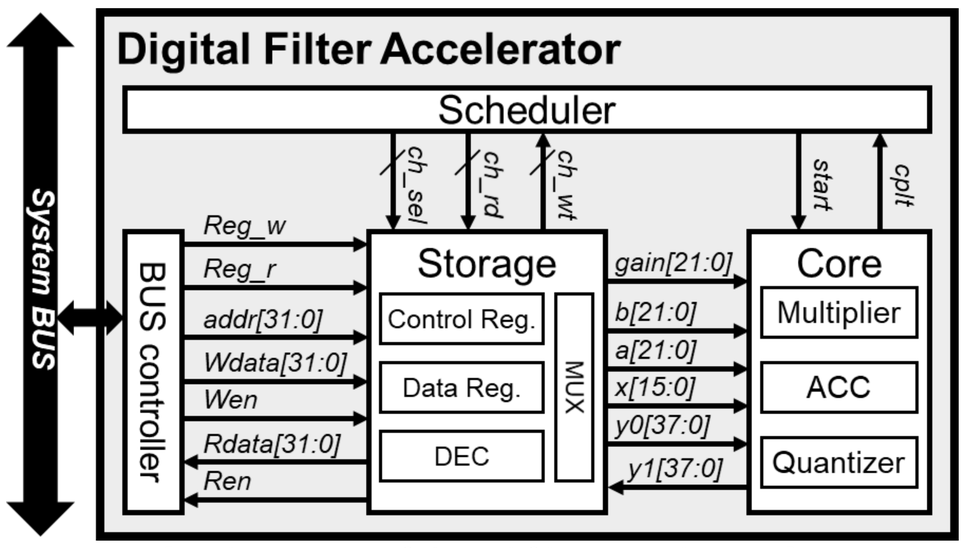
The IIR filter needs fewer orders than the FIR filter for the same design specification because of using the output signal. So IIR filter is more appropriate than the FIR filter. We designed an IIR digital filter based on a fixed-point calculation by 4-channel 1-order filter that can operate up to 4-order. 4 channel 1-order filter has 8 coefficients to multiply, the same as the 4-order filter. 1-order filter can be transformed into various filter structures by exploiting scheduling channels. Also, because input data for each channel can be applied independently, the accelerator is available in the system with a maximum of four sensors.



[Structure of 4-order IIR digital Filter]

Digital Filter Accelerator

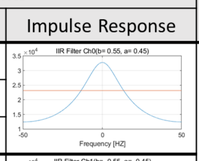
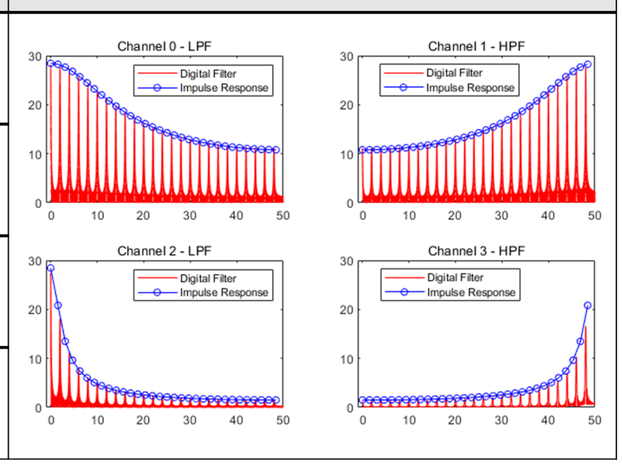
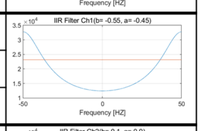
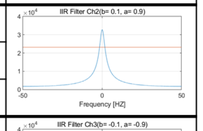
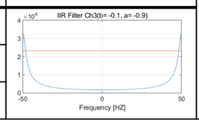
The accelerator consists of scheduler, storage, computation core, and BUS controller. The scheduler controls the data on channels, sends the start command in the core, and detects the completion of the core. The storage includes data about configuration, input/output, and coefficient. The computation core is a fixed-point based IIR filter and computes data pairs like (x0,b0),(y0,a0) in 4 channels assigned by scheduler. When the core completes the computation, it sends the output data into the storage and complete signal into the scheduler.



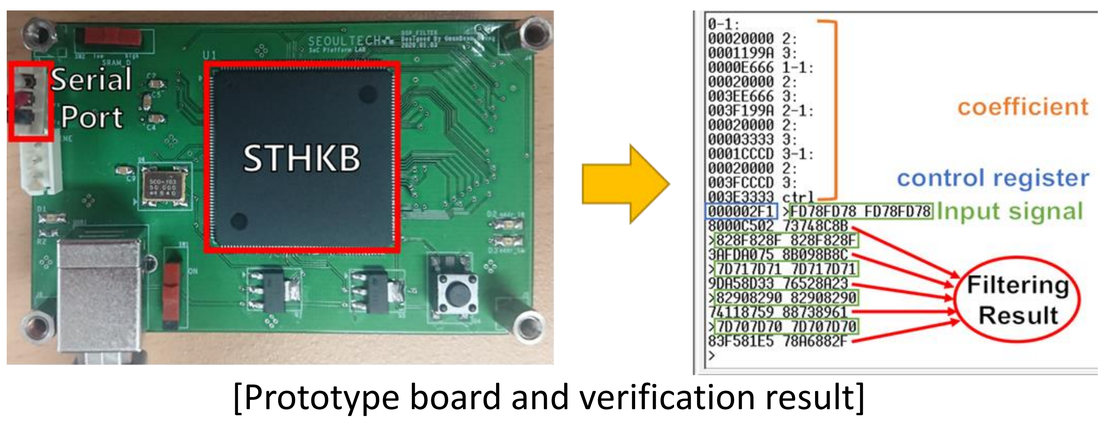
[Architecture of digital filter accelerator]

Chip Verification

We designed a prototype PCB including our chip to verify the digital filter accelerator. In order to configure the accelerator, the main processor requests coefficient data, control data, and input data in sequence through serial communication. After that, the processor sends coefficients and input data to the accelerator, and the accelerator starts filtering. The filtering result output y of each channel is stored into the data register and send back to the core input y. The accelerator transmits the complete interrupt signal when completed all channels that enabled. We verified the chip by confirming the filtering result.

Ch	Coefficients			Impulse Response	Impulse Response of Output Signal
	name	hex (22 bit)	real		
0	gain	020000	1.00		
	b	01199A	0.55		
	a	00E666	0.45		
1	gain	020000	1.00		
	b	3EE666	-0.55		
	a	3F199A	-0.45		
2	gain	020000	1.00		
	b	003333	0.10		
	a	01CCCD	0.90		
3	gain	020000	1.00		
	b	3FCCCD	-0.10		
	a	3F3333	-0.90		

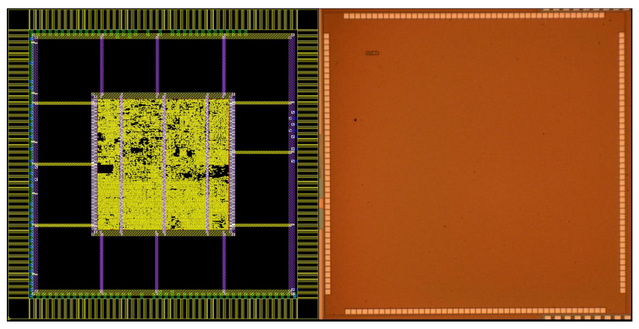
[Impulse response analysis]



[Prototype board and verification result]

Chip Implementation

Chip specifications	
Technology	180nm CMOS
Supply Voltage	3.3 V
Chip Size	3.8 x 3.8 mm^2
Max. Frequency	50 MHz
Gate Counts	191K @ 50 MHz



[Chip Layout and Photograph]

Acknowledgement

The chip fabrication and EDA tool were supported by the IC Design Education Center(IDEC), Korea